Abstract

The TOTEM experiment at the Large Hadron Collider (LHC) at European Organization for Nuclear Research (CERN) measures the total proton-proton cross section with precision of 1%, elastic proton scattering and diffractive dissociation. The performed upgrade of the accelerator during the First Long Shutdown period (LS1) will allow to reach unprecedented collision energy of 13 TeV at the centre-of-mass and higher luminosity. Thus, the physics program of the TOTEM experiment for upcoming runs implies higher requirements for Data Acquisition System (DAQ). The thesis addresses consolidation of the TOTEM DAQ with the Scalable Readout System (SRS) in order to meet the new demands. It covers the full project life: concept, design of the full system architecture, firmware development, hardware tests and an extensive design verification based on the HDL simulation. As the new DAQ utilizes Field-Programmable Gate Array (FPGA) devices, the amount of logic resources gives a possibility of online data processing and effective lossless data compression in order to increase further the performance. The achieved results are more than one order of magnitude higher in terms of trigger rate capabilities with respect to the legacy system. Finally, the thesis demonstrates a hardware implementation of algorithm performing track identification. It introduces idea of building fully in hardware a Second Level Trigger filtering out irrelevant physics events. Uniqueness of this particular approach lies in usage of a full-resolution data available to the algorithm utilizing only limited resources of the programmable devices. The analysis of the possible event topologies and its statistics in the acceptance range of the TOTEM silicon detectors yielded an optimal solution. The conducted performance studies of the implemented algorithm are referred in the thesis.